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**IN THE CLAIMS**

Please amend the claims as follows:

1. (original) A binary coded decimal adder circuit for adding two operands and an input carry to give a sum comprising:

a first stage receiving said operands, grouping said operands into equal length blocks of contiguous bits and, for each said block, logically computing from said operands an intermediate sum vector, an intermediate carry vector, a propagate function and a generate function;

a second stage receiving said input carry and receiving from each said block of said first stage the respective propagate function and generate function, and carry look ahead computing therefrom carries for each said block and an output carry; and

a third stage, having the same number of blocks as said first stage, each third stage block receiving a respective intermediate sum vector, and logically adjusting said intermediate sum vector by pre-correction factors which depend upon a respective intermediate carry vector, at least two of the one of said second stage carries and said input carry; and

wherein outputs of said third stage logic blocks together represent said sum of operands.

2. (original) The adder circuit of claim 1, wherein said blocks are 4-bits in length.

3. (original) The adder circuit of claim 1, wherein said operands are of 16-bit length, and further wherein:

said first stage has a like logic circuit for each 4-bit block;

said second stage has a single carry look ahead logic circuit; and

said third stage has a like sum correction logic circuit for each 4-bit block.

4. (original) The adder circuit of claim 1, wherein said operands are of 64-bit length, and further wherein:

said first stage has a like logic circuit for each 4-bit block;

said second stage has a first carry look ahead level of four carry look ahead logic circuits providing partial carries to a second carry look ahead level of a single carry look ahead circuit; and

said third stage has a like sum correction circuit for each 4-bit block.

5. (original) The adder circuit of claim 1, wherein said pre-correction factors are calculated depending upon four cases of the logical combinations of two carries.

6. (original) The adder circuit of claim 5, wherein said pre-correction factors include the carry from the intermediate carry vector and a bit pattern depending upon the relevant one of said four cases.

7. (original) The adder circuit of claim 1, wherein said intermediate sum vector and said intermediate carry vector are computed by three cascaded Half-Adder circuits.

8. (original) The adder circuit of claim 1, wherein said pre-correction factors include one of four values decided on the basis of a carry from a preceding block and a carry from the current block.

9. (original) A binary coded decimal adder circuit for adding two 4N-bit operands and an input carry to give a sum comprising:

a first stage receiving said operands, grouping said operands into N contiguous 4-bit length blocks and, for each said block, logically computing from said operands an intermediate sum vector, an intermediate carry vector, a propagate function and a generate function;

a second stage receiving said input carry and receiving from each said block of said first stage the respective propagate function and generate function, and carry look ahead computing therefrom carries for each said block and an output carry; and

a third stage, having the same number of blocks as said first stage, each third stage block receiving a respective intermediate sum vector, and logically adjusting said intermediate sum vector by pre-correction factors which depend upon a respective intermediate carry vector, at least two of the one of said second stage carries and said input carry; and

wherein outputs of said third stage logic blocks together represent said sum of operands.

10. (original) The adder circuit of claim 9, wherein said pre-correction factors are calculated depending upon four cases of the logical combinations of two carries.

11. (original) The adder circuit of claim 10, wherein said pre-correction factors include the carry from the intermediate carry vector and a bit pattern depending upon the relevant one of said four cases.

12. (original) The adder circuit of claim 10, wherein said pre-correction factors are calculated from the carry $C_{N-3}$ of the previous 4-bits and the carry $C_{N+1}$ of the current 4-bits.

13. (original) The adder circuit of claim 9, wherein said intermediate sum vector and said intermediate carry vector are computed by three cascaded Half-Adder circuits.

14-19. (canceled)